REMARKS

Amendments made to the specification were purely stylistic and did not introduce any new matter.

Favorable reconsideration and allowance of the application in view of the foregoing amendments to claim 1 and following remarks is respectfully requested. Moreover, the Applicants have reviewed the Office Action of September 22, 2000 and submit that this Amendment is responsive to all points raised therein.

Notice of Draftsperson's Patent Drawing Review

Applicants note the objection of the Draftsperson of all the figures. Applicants request permission to defer submission of formal drawings correcting these objections until the present application is allowed.

Claim Rejections under 35 USC §112

Claims 10 and 11 have been rejected under 35 USC §112, first paragraph. The Office Action states that "a flip flop", "a random number generator" and "an adder" do not commensurate with the drawings. Applicants respectfully draw the Examiner's attention to Figs. 3 and 5, where block 302 is an adder and block 304 is a flip flop. In Fig. 5, block 502 is an adder, and block 500 is a random number generator. Accordingly, Applicants respectfully traverse this rejection and request that it be withdrawn.

In view of the above, Applicant believes that claims 10 and 11 should be allowed.

Claim Rejections under 35 USC §102

Claims 3 – 7 have been rejected under 35 USC §102(b) as being anticipated by Buch (U.S. Patent No. 5,712,636). Applicants respectfully traverse this rejection.

Regarding claim 3, Applicants respectfully disagree with the Office Action's statement that "Buch teaches a device (fig. 1) that comprises ... a controller ... said controller operative to open and close said at least one switch thereby switching the resistance of said low pass filter is inherent (states of the switch: ON and OFF; see abstract)". Buch teaches "a pulse-width-modulated digital-to-analog converter ... responsive to a digital control value for switching between a high gain mode and a low gain mode." In col. 5, lines 25 - 27, Buch

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explicitly states that "in either mode, the impedance of the filter 120 remains constant." Impedance is a vector quantity consisting of two independent scalar phenomena: resistance and reactance. Clearly, if the impedance of the filter 120 remains constant, then the resistance of the filter 120 remains constant as well. Buch therefore fails to disclose all elements of claim 3, and Applicants respectfully request that this rejection be withdrawn.

Regarding claim 4, Applicants respectfully disagree with the Office Action's statement that "Buch teaches a device (fig. 1) that comprises ... a controller ... said controller operative to open and close said at least one switch thereby changing said response time (fig. 1)". In col. 5, lines 27 - 28, Buch explicitly states that "Therefore the filter's time constant will also remains constant." Buch therefore fails to disclose all elements of claim 4, and Applicants respectfully request that this rejection be withdrawn.

Regarding claims 5 - 7, Applicants respectfully disagree with the Office Action's statement "Buch teaches a digital to analog converter (fig. 1) that comprises ... a switchable low pass filter (120, fig. 1) having a plurality of response times". As explained above with respect to claim 4, the filter's time constant, and therefore its response time, remains constant in Buch's device. The filter of Buch's device therefore does not have a plurality of response times. Buch therefore fails to disclose all elements of claim 5, and fails to disclose all elements of its dependent claims 6 and 7, and Applicants respectfully request that this rejection be withdrawn.

Claim Rejections under 35 USC §103

Claims 1, 2, 8 and 9 have been rejected under 35 USC §103 as being unpatentable over Buch (U.S. Patent No. 5,712,636). Applicants respectfully traverse this rejection.

As pointed out above, the circuit according to the Bush reference has a fixed effective resistance and, therefor, a fixed time constant. "Both the path 85 and the path 90 of the resistive network 81 are driven in parallel.."[Bush: Col. 4, Lines 14-16] and "the output impedance of the filter remains substantially constant. Therefore, the filter's time constant will also remain constant"[Bush: Col. 2, Lines 52 - 54]. It would go against the teachings of Bush to incorporate a second switch, as the Examiner has suggested would be obvious, and to switch the effective resistance and the time constant of the Bush circuit.

Applicants have amended claim 1 in order to add a limitation of "alter[ing] the

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effective resistance of said switchable low pass filter." Amended claim 1 and original claims 8 and 9 each contain limitations relating to either an altering of the circuit's effective resistance or the circuit's time constant. This limitation is neither taught nor suggested in the Bush reference. As a matter of fact, the Bush reference teaches away from altering its circuit's effective resistance or time constant. Therefore, Applicants respectfully request allowance of claims 1, 8 and 9, and all claims depending therefrom.

Conclusion

Applicants believe they have conclusively and positively addressed all the substantive issues raised by the Examiner's Office Action of September 20, 2000. Applicants therefore request allowance of all pending claims and an issuance of a "Notice of Allowance" for this application.

The Draftsman's objections to the drawings will be addressed immediately after a "Notice of Allowance" is issued.

If the Examiner has any questions or comments as to this paper, the Examiner is requested to contact the undersigned at the address and telephone number below.

Respectfully submitted,

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VERSIONS WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The section "SUMMARY OF THE INVENTION" beginning at page 4, line 1 and ending at page 6, line 13 has been deleted.

Paragraph beginning at line 6 of page 7 has been amended as follows:

Fig. 1 is a schematic illustration of a portion of an integrated circuit having a DAC of [a preferred] an embodiment of the present invention implemented in it;

Paragraph beginning at line 13 of page 7 has been amended as follows:

Fig. 3 is a schematic illustration of the digital converter of Fig. 1, according to [a preferred] an embodiment of the present invention;

Paragraph beginning at line 17 of page 7 has been amended as follows:

Fig. 5 is a schematic illustration of a modified version of the digital converter of Fig. 3, according to [a preferred] an embodiment of the present invention.

Paragraph beginning at line 6 of page 8 has been amended as follows:

Reference is now made to Fig. 1, which is a schematic illustration of a portion of an integrated circuit 100, having a DAC of [a preferred] an embodiment of the present invention implemented in it. Reference is made additionally to Fig. 2A, which is an exemplary graphical illustration of a pulse modulated signal as a function of time, and to Figs. 2B, 2C and 2D, which are exemplary graphical illustrations of the output analog signal of Fig. 1 as a function of time. In Figs. 2B, 2C and 2D, the horizontal line 201 indicates the desired constant analog signal.

Paragraph beginning at line 23 of page 9 has been amended as follows:

According to [a preferred] an embodiment of the present invention, the DAC achieves a fast response time and a small ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will

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charge in the fast response mode. This is shown in Fig. 2C by the solid-line graph 206. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2C by the dotted-line graph 208. In such a way, the DAC takes advantage of the fast response mode while the capacitor C is charging, and takes advantage of the small ripple mode when the capacitor C is close to or already at the desired voltage level. As a result, the DAC of the present invention produces a far more stable analog control signal than that of a conventional pulse modulated DAC.

Paragraph beginning at line 12 of page 10 has been amended as follows:

According to another [preferred] embodiment of the invention, the DAC achieves a fast response time and no ripple in the steady-state. When the multi-bit digital signal changes, resulting in a new single bit digital signal, the controller 106 closes switch SW1 and opens switch SW2 so that the capacitor C will charge in the fast response mode. This is shown in Fig. 2D by the solid-line graph 210. When the capacitor C reaches the desired voltage level at time T_1, the controller 106 opens switch SW1 and closes switch SW2 so that the capacitor C will retain its desired voltage level with a small ripple. This is shown in Fig. 2D by the dotted-line graph 212. When a no-ripple, very stable analog signal is required at beginning at time T_3, the controller 106 opens both switches SW1 and SW2 so that the capacitor C will retain its voltage level in hold mode. This is shown in Fig. 2D by the almost flat dashed line 214.

Paragraph beginning at line 24 of page 10 has been amended as follows:

The motivation for this [preferred] embodiment is that there are cases, such as control signals for time division multiple access (TDMA) applications, where a very stable, slowly decreasing signal is preferable to even a small ripple. In such applications, the controller is set so that the time T_3 precedes or substantially coincides with the time at which the analog control signal is needed.

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Paragraph beginning at line 5 of page 11 has been amended as follows:

A further advantage of this [preferred] embodiment is that during hold mode, the switchable LPF 104 draws no current, and the digital converter 102 can be turned off, resulting in a reduction in the overall power consumption.

Paragraph beginning at line 10 of page 11 has been amended as follows:

The operation of the digital converter 102 of Fig. 1 will now be explained with respect to Figs. 3 and 4, to which reference is now made. Fig. 3 is a schematic illustration of a pulse density modulation (PDM) digital converter, according to [a preferred] an embodiment of the present invention.

Paragraph beginning at line 24 of page 11 has been amended as follows:

According to a further [preferred] embodiment of the present invention, the DAC spreads the spectral properties of the harmonic ripple using random noise. As is known in the art, a PDM signal is composed of pulses whose density is proportional to the value of the multi-bit digital input signal. The frequency of these pulses, known as the ripple frequency, appears in the output analog signal and interferes with the desired signal. The same problem occurs with the output analog signal of a PWM signal, although its ripple frequency is generally lower than that generated by a PDM signal. In [the further preferred] this embodiment of the present invention, the timing of the pulses in the pulse modulated signal is adjusted by a small, random factor, thereby spreading the spectral properties of the harmonic ripple. Reference is now made additionally to Fig. 5, which is a schematic illustration of a modified version of the digital converter of Fig. 3, according to a further [preferred] embodiment of the present invention. In addition to the adder 302 and the flip-flop 304, the digital converter 102 comprises a uniform distribution random number generator 500 and an additional adder 502. The random number generator 500, for example a pseudo-random number (PN) generator, which is known in the art, is driven by a clock 504. For each cycle of the clock 504, the random number generator 500 generates a random number in the range –M to +M, where M is significantly smaller than N. The adder 502 adds the random number to the value in

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the flip-flop 304, and the result is added by the adder 302 to the N-bit digital signal input. The resulting pulse modulated signal is shown in Fig. 4 by the dashed-line graph. The effect is that the pulses generated by the digital converter of Fig. 5 are slightly offset in time ("jittered") from the pulses generated by the digital converter of Fig. 3. Sometimes, as in pulse 400, the two signals are coincident, sometimes, as in pulse 402, the jittered signal is early, and sometimes, as in pulse 404, the jittered signal is late. Introducing a small random noise into the pulse modulated signal spreads the spectral properties of the pulse frequency (which is the ripple frequency of the analog output signal produced by low pass filtering of the pulse modulated signal).

In the claims:

1. (Amended) A switchable low pass filter comprising:

a first switch connected to a first resistive element;

a second switch connected to a second resistive element;

a capacitive element connected to said first resistive element and to said second resistive element; and

a controller [connected] coupled to said first switch and said second switch, said controller [operative] adapted to alter the effective resistance of said switchable low pass filter by opening or closing either of said switches.[to open and close at least one of said first switch and said second switch.]

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